Remarks

Claims 3 to 20, as amended, are presented for reconsideration.

Claims 1 and 2 are cancelled.

Claim 3 has been amended to conform with language agreed to between the Undersigned and Examiner Le in a telephone interview conducted January 4, 2006.

Claims 10, 11, 12, 19 and 20 have been amended to overcome the rejection based on 35 U.S.C. 112, second paragraph. As for Claims 10 to 12, the recited transfer transistor and transfer gate are represented in the Drawing as element TX1 or element TX2, for example, and the claims now recite a transfer gate transistor. Claims 19 and 20 have been amended to be consistent with language in Amended Claim 3.

The title has been amended to be more descriptive, and a minor spelling correction is being made in the first paragraph of the specification.

Claims 3 - 5, 8, 10 - 12, 14 and 15 - 20 were rejected under 35 U.S.C. § 102 (e) as being allegedly anticipated by Gowda et al. Claims 2, 6, 7, 9 and 13 (as understood) were rejected under 35 U.S.C. § 103(a) as being allegedly obvious and unpatentable over Gowda et al.

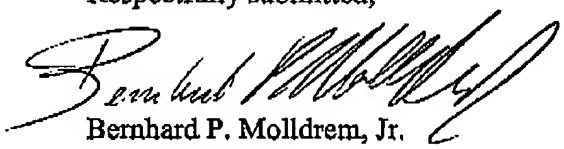
Claim 3, as amended, and its dependent claims focus on the main aspect this invention, namely, grouping the pixel elements so that the array of pixels is considered a multiplicity of pixel groups, e.g., double pixels (Figs. 4, 5, 6, 8 or 9) or quadruple pixels (Figs. 10, 11). Each pixel group has one output transistor (e.g., 60) that is shared with the first and second pixel photosensitive elements (e.g., 53 and 57), and each group also has one reset transistor (e.g., 62) that is shared between the first and second pixel photosensitive elements. The first and second elements both have their output electodes coupled together to the sense electrode of the shared output transistor (e.g., 60). This architectural feature allows for lower cost and higher pixel density, because it allows the number of transistors to be reduced to only two per pixel (i.e., four transistors per two-pixel group).

By contrast, in the cited Gowda et al. reference the pixels are not grouped; there is one reset FET (e.g., 21) and one pixel amplifer (e.g., 23) for each photosensivive element (e.g., 26), in addition to the row select FET (22). Throughout the many embodiments shown in the Gowda

et al. reference, there is always a minimum of three transistors per pixel, i.e., per photosensitive element. The Gowda approach does no better than the three-transistor (per pixel) limit discussed in the background section of this application, e.g., page 2, line 20 to line 28.

It is urged that all of Claims 3 to 20, as now asserted, are patentable, and early and favorable consideration is solicited.

Respectfully submitted,



Bernhard P. Molldrem, Jr.
Reg. No. 28,973
Attorney for Applicant

224 Harrison Street
Syracuse NY 13202
(315) 422-4323
fax - (315) 422-4318